**In the Claims**:

Claims 1-10 (Cancelled).

11. (New) A method for programming an electronic memory device comprising a plurality of non-volatile memory cells each having a conduction terminal associated therewith, a voltage regulator having at least one input and an output, and a conductor having a first end connected to the output of the voltage regulator and a second end connected to a common circuit node also connected to each of the conduction terminals, the method comprising:

outputting a first voltage from the output of the voltage regulator to the first end of the conductor, the conductor having a parasitic intrinsic resistance associated therewith; and

feeding back a second voltage from the common circuit node along a feedback path to the at least one input of the voltage regulator.

12. (New) The method of Claim 11 wherein the feedback path comprises a resistor and also has a parasitic feedback path resistance associated therewith.

13. (New) The method of Claim 11 wherein the at least one input comprises an inverting input and a non-inverting input, wherein the feedback path is connected to the inverting input, and wherein the non-inverting input is connected to a reference voltage.

14. (New) The method of Claim 11 further comprising buffering the first voltage between the output of the voltage regulator and the common circuit node.

15. (New) The method of Claim 11 wherein the non-volatile memory cells comprise multi-level non-volatile memory cells.

16. (New) The method of Claim 11 wherein the conductor comprises a metal line.

17. (New) A method for supplying power to a load from among a plurality of loads each connected to a conductor having first and second ends, the method comprising:

applying a first voltage to the first end of the conductor using a voltage regulator, the voltage regulator having at least one input and an output and being connected to the first end of the conductor at the output, and the conductor having at least one routing resistance associated therewith; and

feeding back a second voltage from the second end of the conductor along a feedback path to the at least one input of the voltage regulator.

18. (New) The method of Claim 17 wherein the loads are spaced apart along the conductor, and wherein the at least one routing resistance comprises a plurality of routing resistances each associated with a respective load.

19. (New) The method of Claim 17 wherein the feedback path has a parasitic resistance associated therewith.

20. (New) The method of Claim 17 wherein the conductor comprises a metal line.

21. (New) An electronic memory device comprising:

a programming circuit having at least one input and an output;

a plurality of non-volatile memory cells each having a conduction terminal associated therewith;

a conductor having a first end connected to the output of said programming circuit and a second end connected to a common circuit node, the common circuit node also being connected to each of the conduction terminals, the conductor having a parasitic intrinsic resistance associated therewith; and

a feedback path connected between the common circuit node and the at least one input of said programming circuit.

22. (New) The electronic memory device of Claim 21 wherein said programming circuit comprises a voltage regulator.

23. (New) The electronic memory device of Claim 21 wherein said feedback path comprises a resistor and also has a parasitic feedback path resistance associated therewith.

24. (New) The electronic memory device of Claim 21 wherein the at least one input comprises an inverting input and a non-inverting input, wherein said feedback path is connected to the inverting input, and wherein the non-inverting input is connected to a reference voltage.

25. (New) The electronic memory device of Claim 21 further comprising a buffer connected to the output of said programming circuit.

26. (New) The electronic memory device of Claim 21 wherein said non-volatile memory cells comprise multi-level non-volatile memory cells.

27. (New) The electronic memory device of Claim 21 wherein said conductor comprises a metal line.

28. (New) The electronic memory device of Claim 21 wherein each memory cell comprises at least one floating gate transistor having a source terminal, a drain terminal, and a gate terminal, and wherein the drain terminal of each floating gate transistor is connected to the common circuit node.

29. (New) The electronic memory device of Claim 21 wherein said programming circuit, said non-volatile memory cells, said conductor, and said feedback path are implemented in a semiconductor device.